Computer Organization

Part 22 : Main Memory Organization - RAM

UNIT – IV

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RAM Cell

Fig. 6.8 TTL RAM CELL
MOS SRAM Cell

Fig. 6.9 MOS static RAM cell
RAM Using 2D Decoding
Dynamic RAM

From Computer Desktop Encyclopedia
DRAM Write Operation

(a) Writing a 1 into the memory cell

(b) Writing a 0 into the memory cell
DRAM Read Operation

Fig. 6.16 (a) Reading a 1 from the memory cell
DRAM Refresh Operation

(b) Refreshing a stored 1
DRAM Memory Organization
# SRAM vs. DRAM

<table>
<thead>
<tr>
<th>SRAM</th>
<th>DRAM</th>
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<tbody>
<tr>
<td>Less memory cells per unit area</td>
<td>More memory cells per unit area</td>
</tr>
<tr>
<td>Less access time hence faster</td>
<td>Access time is fast</td>
</tr>
<tr>
<td>Consisting flip-flop</td>
<td>Contains MOSFET and capacitor</td>
</tr>
<tr>
<td>Refreshing circuitry is not required</td>
<td>Refreshing is required</td>
</tr>
<tr>
<td>Costly</td>
<td>Less cost</td>
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</tbody>
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Synchronous DRAM
SDRAM Timing Diagram
Performance Measures

• Memory Latency Time
  – The amount of time taken to transfer a word of data to or from the memory.

• Memory Bandwidth
  – Number of bits or bytes that can be transferred in one second.
DDR SDRAM
Rambus RDRAM

• 500 Mbps data rate
• Vertically mounted DRAMs
• Physically constrained bidirectional bus
• Reduced Voltage swing
• Synchronous Design
• Dual Bank row caching
• High Latency
• Need to incorporate macros of bus interface
• Byte serial to word parallel conversion delay
Chip Packaging

DIP
Chip Packaging

SOJ
Chip Packaging

TSOP
Chip Packaging

Chip Scale Package
Chip Packaging

PGA
Reference

• Computer Architecture and Organization
  – By A. P. Godse

• Computer Organization
  – By John Hayes